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EXAMINER	
KILDAY, LISA A	

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2829	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/632,425	Applicant(s) GEIGER ET AL.	
	Examiner Lisa A Kilday	Art Unit 2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *RCE filed on 4/14/03* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) *20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19 and 21-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

Election/Restrictions

Claim 20 is withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to a nonelected system, there being no allowable generic or linking claim. Applicant timely traversed the restriction (election) requirement in Paper No. 8.

Specification

35 U.S.C. 112, first paragraph, requires the specification to be written in "full, clear, concise, and exact terms." The specification is replete with terms, which are not clear, concise and exact. The specification should be revised carefully in order to comply with 35 U.S.C. 112, first paragraph. Examples of some unclear, inexact or verbose terms used in the specification are: Claim 1 provides that the surface sensitive silicon oxide has a wet etch rate greater than about 6000 Å/min. and that the porous Silicon oxide is deposited at a temperature of less than 400C. However, both the Surface sensitive and Porous Silicon oxide have a wet etch rate greater than about 6000 Å/min (see Table 2). On pg. 4, lines 25-28, the deposition temperature of the porous Silicon oxide are less than 400C. On pg. 19, lines 5-11, the deposition temperature of the Surface sensitive Silicon oxide is between 200-400C, preferably about 380C. Claim 1 contains limitations that are not exclusive to either type of Silicon oxide.

The amendment filed 11/7/02 is objected to under 35 U.S.C. 132 because it introduces new matter into the disclosure. 35 U.S.C. 132 states that no amendment shall introduce new matter into the disclosure of the invention. The added material, which is not supported by the original disclosure, is as follows: "partially filling." The

specification only supports completely filling the gap. Furthermore, the specification discloses that the film has good gap fill properties (pg. 4, lines 13-15). Partially filling the gap would be repugnant to the layer's intended purpose.

Applicant is required to cancel the new matter in the reply to this Office Action.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 1-19, 21-26 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter, which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Claim 1 provides that the surface sensitive silicon oxide has a wet etch rate greater than about 6000 Å/min. and that the porous Silicon oxide is deposited at a temperature of less than 400C. However, both the Surface sensitive and Porous Silicon oxide have a wet etch rate greater than about 6000 Å/min (see Table 2). On pg. 4, lines 25-28, the deposition temperature of the porous Silicon oxide are less than 400C. On pg. 19, lines 5-11, the deposition temperature of the Surface sensitive Silicon oxide is between 200-400C, preferably about 380C. Claim 1 & 25 contains limitations that are not exclusive to either type of Silicon oxide.

In re claim 10, the specification teaches that the PECVD Silicon oxide is the same as the thermal CVD Silicon oxide. See table 1 & 2; pg. 16, lines 9-19; pg. 18, lines 3-15. Applicant also states in the specification that the thermal CVD values are the same as Prior Art (pg. 16, lines 13-15).

Claims 25-6 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter, which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Claim 25 recites the limitation of "partially filling the at least one gap". However, the specification and drawings only support completely filling the at least one gap. Furthermore, the specification discloses how the insulating materials have "good gap fill capabilities" (pg. 4, lines 13-15).

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

Claim 19 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 19 recites the limitation "said silicon oxide" in line 1. There is insufficient antecedent basis for this limitation in the claim.

The term "said silicon oxide" in claim 19 is a relative term, which renders the claim indefinite. The term "said silicon oxide" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one

of ordinary skill in the art would not be reasonably apprised of the scope of the invention. Claim 19 depends on independent claim 10. In claim 10, there are two different types of "silicon oxide." Applicant needs to point out whether the "said silicon oxide" refers to the PECVD silicon oxide or thermal CVD silicon oxide.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-2, 4-7, 9, 23-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cho (5,804,509) and Kwok et al. ("Surface related phenomena in Integrated PECVD/Ozone-TEOS SACVD Processes for sub-half micron gap fill: electrostatic effects", J. Electrochem. Soc., vol. 141, no. 8, Aug. 1994).

In re claim 1, Cho teaches a method for forming an insulation layer over a substrate, the method comprising: forming a surface sensitive silicon oxide layer (3) over the substrate (1); and forming a porous Silicon oxide layer (4) on the Surface sensitive silicon oxide layer (fig. 1) by thermal chemical vapor deposition, wherein said porous silicon oxide layer is deposited at a temperature of about 400C or less (col. 2 lines 50-60). However Cho does not teach wherein the porous silicon oxide layer has a wet etch rate of greater than about 6,000 Å/min. However, Kwok et al. teaches wherein the porous silicon oxide layer has a wet etch rate of greater than about 6,000 Å/min (pg. 2172 col. 2 lines 22-25, table IV, figs. 1-6). Therefore, it would be obvious to one skilled

in the art at the time of the invention to form a porous silicon oxide layer with a wet etch rate of greater than about 6,000 Å/min because it is well known in the art to deposit a porous Silicon oxide layer with an etch rate of 6,000 Å/min.

In re claim 2, Cho discloses the method of claim 1 wherein the porous silicon oxide layer has a carbon content of at least 5 atomic percent. It is inherent that an insulating film formed by a carbon containing silane, Tetraethylorthoxisilicate gas (TEOS), contains a carbon content of at least 5 atomic %.

In re claim 4, Kwok et al. teaches the method of claim 1 wherein the surface sensitive silicon oxide layer is deposited from a plasma enhanced CVD reaction of TEOS and oxygen (title, abstract, table IV).

In re claim 5, Cho teaches the method of claim 1 wherein the porous silicon oxide layer is deposited from a process gas comprising TEOS and ozone (col. 3 lines 53-60).

In re claim 6, Cho teaches the method of claim 5 wherein a molar ratio of said TEOS to ozone is between about 10:1 and 20:1 (col. 3 lines 7-15).

Claim 7 adds the limitation of forming a capping silicon oxide layer over the porous silicon oxide layer. Cho does not teach forming a capping layer over the porous silicon oxide layer. Kwok et al. teaches forming a capping layer over the porous silicon oxide layer (fig. 10). Therefore, it would be obvious to one skilled in the art to form a capping layer over the porous silicon oxide layer because in order to protect the porous silicon oxide during planarization.

In re claim 9, Cho teaches the method of claim 1 wherein said surface sensitive and porous silicon oxide layers are deposited in an in situ process (abstract lines 9-13).

In re claim 23, Cho teaches wherein the substrate (1) includes at least one gap (fig. 1), and wherein the surface sensitive silicon oxide layer (3) partially fills the at least one gap. See 112 rejections above.

In re claim 24, Cho teaches wherein the substrate (1) includes at least one gap (fig. 1), and wherein the porous silicon oxide layer (4) partially fills the at least one gap.

Claims 3, 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cho and Kwok et al. as applied to claim 1 above, and in view of Lan (6,180,507).

In re claim 3, Cho teaches forming a surface sensitive silicon oxide layer over the substrate and a porous silicon oxide layer on the surface of the sensitive silicon oxide layer. Kwok et al. teaches wherein the porous silicon oxide layer has a wet etch rate of greater than about 6,000 Å/min (pg. 2172 col. 2 lines 22-25, table IV, figs. 1-6). However, neither Cho nor Kwok et al. teaches that the porous silicon oxide layer has a dielectric constant of between about 2.9 and 3.2. However, Lan teaches that the dielectric constant of porous silicon oxide layers are (208) between the dielectric constant of air 1.00059 and lower than the dielectric constant of a conventional silicon oxide layer, 4.0 (col. 3 lines 8-15). Therefore, it would be obvious to one skilled in the art to form a porous silicon oxide layer with a dielectric constant of between 2.9 and 3.2 because air in the holes of the porous silicon oxide layer reduce the dielectric constant in order to reduce RC delay. And, it would have been obvious to use silicon oxide with the etch rate of Kwok because it is well known in the art to deposit silicon oxide with an etch rate of 6,000 Å/min.

In re claim 8, Cho teaches the process of claim 1 wherein said porous silicon oxide layer is deposited. However, Cho does not teach using an SACVD process at a pressure of between 100-700 Torr. However, Lan teaches forming a porous silicon oxide layer (212) using TEOS and ozone at a pressure of 100-700 Torr (col. 2 lines 56-61). Therefore, it would be obvious to one skilled in the art to deposit porous silicon oxide layer at sub-atmospheric pressure in order for uniform and controlled deposition.

Claims 10-19, 21-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cho and Kwok in view of Lan.

In re claim 10, Cho teaches a method for depositing an intermetal dielectric film over a plurality of conductive lines (2). However, Cho does not teach depositing a plasma enhanced chemical vapor silicon oxide. Kwok teaches a method comprising: depositing a plasma enhanced chemical vapor deposition (CVD) silicon oxide layer (col. 2 lines 30-35, table II) over the plurality of conductive lines from a plasma of tetraethyloxysilane (TEOS) and oxygen (fig. 5); and depositing a silicon oxide layer over the plasma enhanced CVD silicon oxide layer by a thermal CVD process from a gas mixture of a TEOS and ozone (pg. 2174 col. 1 lines 15-20). Therefore, it would have been obvious to one of ordinary skill at the time of the invention to modify the process of Cho by depositing PECVD silicon oxide to reduce the stress hysteresis of the silicon oxide layer. However, neither Cho nor Kwok does not teach that said thermal silicon oxide layer has a dielectric constant of about 3.2 or less. It is inherent that an insulating film formed by a carbon containing silane, Tetraethylorthoxisilicate gas (TEOS), contains a carbon content of at least 5 atomic %. However, Lan teaches that

the dielectric constant of porous silicon oxide layers (208) are between the dielectric constant of air 1.00059 and lower than the dielectric constant of a conventional silicon oxide layer, 4.0 (col. 3 lines 8-15). Therefore, it would be obvious to one skilled in the art to form a porous silicon oxide layer with a dielectric constant of between 2.9 and 3.2 because air in the holes of the porous silicon oxide layer reduce the dielectric constant in order to reduce RC delay.

Claim 11 adds the limitation of wherein the density of said thermal silicon oxide layer is less than or equal to about 1.7 g/cm3. Cho teaches that the density of the thermal silicon oxide layer is less than or equal to about 1.7 g/cm3 (col. 5 lines 21-25).

Claim 12 adds the limitation of forming a PECVD silicon oxide layer capping over the thermal silicon oxide layer. Cho does not teach forming a capping layer over the thermal silicon oxide layer. However, Lan teaches forming a capping layer (214) over the thermal silicon oxide layer (208). Therefore, it would be obvious to one skilled in the art to form a capping layer over the thermal silicon oxide layer because the capping layer protects the thermal silicon oxide layer.

In re claim 13, Cho teaches forming a thermal silicon oxide layer. However, Cho does not teach that the dielectric constant of said thermal silicon oxide layer is greater than or equal to about 2.9. However, Lan teaches that the dielectric constant of porous silicon oxide layers are (208) between the dielectric constant of air 1.00059 and lower than the dielectric constant of a conventional silicon oxide layer, 4.0 (col. 3 lines 8-15). Therefore, it would be obvious to one skilled in the art to form a porous silicon oxide

layer with a dielectric constant that is greater than or equal to about 2.9 and 3.2 because air in the holes of the porous silicon oxide layer reduce the dielectric

Claims 14-16 adds the limitation of wherein a molar ratio of said TEOS and ozone used to deposit said thermal silicon oxide layer is at least 8:1. Cho teaches that a molar ratio of said TEOS and ozone used to deposit said thermal silicon oxide layer is at least 8:1 (col. 3 lines 7-15) and in the range of 10:1-20:1. However Cho does not teach the limitation of claim 10, wherein the thermal silicon oxide layer has a dielectric constant of about 3.2 or less. Lan teaches depositing a thermal oxide layer with TEOS and ozone with a dielectric constant that is lower than the conventional silicon oxide layer. It would be obvious to one skilled in the art to deposit a thermal silicon oxide layer with a molar ratio of TEOS to O3 that is greater than 8:1 but in the range of 10:1 and 20:1 as a matter of routine optimization.

Claim 17 adds the limitation of wherein said oxygen is provided from a flow of molecular oxygen. Cho does not teach providing a molecular oxygen source. However, Lan teaches forming a thermal CVD layer using a molecular oxygen source as a source of oxygen (col. 2 lines 56-60). It is well known in the art to use molecular oxygen as the source of oxygen. Therefore, it would be obvious to one skilled in the art to deposit a thermal silicon oxide layer using molecular oxygen as a source for oxygen in addition to TEOS or ozone because molecular oxygen is an inexpensive source of oxygen and well-known substitute for O3 or TEOS.

Claim 18 adds the limitation of wherein said plasma enhanced and thermal CVD silicon oxide layers are deposited in an in situ process. Kwok teaches forming PECVD

and thermal CVD silicon oxide layers in situ (abstract lines, title, pg. 2172 lines 40-50). However, Kwok does not teach forming a low dielectric constant layer. However Lan teaches forming CVD layers that have a low dielectric constant layer. It is well known in the art to form silicon oxide layers in situ. Therefore, it would be obvious to one skilled in the art to form PECVD and thermal silicon oxide layers in situ as taught by Kwok et al. in order to reduce the dielectric constant as taught by Lan.

In re claim 19, Cho teaches the process of claim 10 wherein said porous silicon oxide layer is deposited. However, Cho does not teach using an SACVD process at a pressure of between 100-700 Torr. However, Lan teaches forming a porous silicon oxide layer (212) using TEOS and ozone at a pressure of 100-700 Torr (col. 2 lines 56-61). Therefore, it would be obvious to one skilled in the art to deposit porous silicon oxide layer at sub-atmospheric pressure in order for uniform and controlled deposition.

In re claim 21, Cho does not teach wherein the plasma enhanced CVD silicon oxide layer partially fills gaps between the plurality of conductive lines. However, Kwok teaches forming plasma enhanced CVD silicon oxide (abstract) to partially fills gaps between the plurality of conductive lines (pg. 2172 col. 1 lines 14-25). Therefore it would be obvious to one skilled in the art to form plasma enhanced CVD silicon oxide to partially fills gaps between the plurality of conductive lines in order to promote gap fill capability.

In re claim 22, Cho does not teach wherein the thermal silicon oxide layer partially fills gaps between the plurality of conductive lines. However, Lan teaches forming thermal silicon oxide (212) to partially fill gaps between the plurality of

conductive lines (fig. 2E, col. 3 lines 39-41). Therefore it would be obvious to one skilled in the art to form thermal silicon oxide to partially fills gaps between the plurality of conductive lines in order to prevent cross talk between metal lines to improve quality of the devices.

Response to Arguments:

Applicant is basing their specification and invention on prior art of Kwok. However, applicant fails to distinguish their invention by teaching a novel and non-obvious invention. Applicant argues on pg. 5 of their response, that Kwok fails to teach a surface sensitive silicon oxide layer with a wet etch rate of greater than about 6000 Å/min. However, applicant admits that Kwok discloses a wet etch rate of 10,000Å/min. or greater for a thermal oxide film and PECVD (PE-TEOS) oxide. However, this point is moot because 10,000 is greater than 6,000. Kwok's teachings read on the instant application. Applicant's representative citing of *In re Waymouth* is moot because this decision relied on the facts that the disputed limitation was a range. In this instant case, *In re Waymouth* does not apply because the claimed wet etch rate is greater than 6,000 Å/min, not a range. This value includes 10,000 Å/min. Any value over 6,000 Å/min would suffice.

Applicant argues the critical features of 6,000 Å/min such as: reduced density, and reduced dielectric constant. Applicant's point is moot because those limitations are not found in the claims.

Applicant argues that there is no motivation for Cho to form the insulating layer at a wet etch rate greater than about 6000Å/min. Cho teaches in fig. 1A forming a porous

silicon oxide layer (4) on the surface sensitive silicon oxide layer (3). Cho does not teach wherein porous silicon oxide layer has a wet etch rate of greater than about 6000 Å/min. However, Kwok teaches forming a porous silicon oxide layer has a wet etch rate of greater than about 6000 Å/min (pg. 2172 col. 2 lines 22-25, table IV, figs. 1-6). Therefore, it would be obvious to one skilled in the art at the time of the invention to form a porous silicon oxide layer with a wet etch rate of greater than about 6,000 Å/min because it is well known in the art to deposit a porous Silicon oxide layer with an etch rate of 6,000 Å/min.

Claims 3, 8, 10-19 are unpatentable over Cho and Kwok et al. in view of Lan. Lan teaches that the dielectric constant of porous silicon oxide layer is lower than that of conventional silicon oxide (col. 3 lines 8-15). Applicant argues that Lan fails to teach a porous silicon oxide layer on the surface sensitive silicon oxide layer wherein the surface sensitive silicon oxide layer has a wet etch rate of greater than about 6,000 Å/min. Lan's layer –208- of porous silicon oxide is a dielectric layer. The porous silicon oxide layer contains air; the air holes are what make this layer (208) porous. The dielectric constant of a conventional silicon oxide layer is 4.0 – 4.9. The dielectric constant of air is 1.00059. The dielectric constant of porous silicon oxide is in the range of 1.00059 – 4.0. Therefore, the dielectric constant of porous silicon oxide is taught to be on the claimed layer.

Lan teaches forming a porous silicon oxide layer (212). Lan teaches that the porous silicon oxide layer (212) consists of two portions: a porous silicon oxide (208) and a dense silicon oxide (210) (col. 2 lines 62-64). Therefore it would be obvious to

one skilled in the art to form different types of silicon oxide due to different bonding situations (col. 3 lines 1-7). Cho teaches forming a porous silicon oxide layer (4) on a surface sensitive oxide layer (3). Kwok et al. teaches wherein the porous silicon oxide layer has a wet etch rate of greater than about 6000 Å/min. Furthermore, applicant is aware that this etch rate is well known because the Applicant's Admitted Prior Art (APA) teaches that a porous silicon oxide layer has a wet etch rate of greater than about 6000 Å/min is well known in the art. See pg. 17 lines 13-19, table 2. Cho has the benefit of a preferred method, which fills the gaps with homogenous step coverage and prevents voids due to the penetration of moisture (col. 1 lines 50-54).

Conclusion

Any inquiry of a general nature or relating to the status of this application should be directed to the Group Receptionist whose telephone number is (703) 308-0957. See MPEP 203.08.

Any inquiry concerning this communication from the examiner should be directed to Lisa Kilday whose telephone number is (703) 306-5728. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo, can be reached on (703) 308-1233. The fax number for the group is (703) 305-3432. MPEP 502.01 contains instructions regarding procedures used in submitting responses by facsimile transmission.

Lisa Kilday

LAK

5/2/03

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